

Apple, No. 10/023,825
Reply to Office action of 09/17/2003

REMARKS/ARGUMENTS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 2-4 and 13 are pending in this case. Claims 2-4 are amended herein and claims 1 and 5-12 are cancelled herein. Claim 13 is added herein.

The Examiner objected to the Abstract because it fails to fall within the range of 50-150 words. A new Abstract is provided herein to comply with the 50-150 word range.

The Examiner objected to claim 1 due to informalities. Claim 1 is cancelled and replaced by claim 13 to overcome the objection.

The Examiner rejected claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Ma et al. (U.S. 4,855,247) or Huang (U.S. 4,963,504; with particular emphasis to claim 1 in Huang) or Sanchez (U.S. 5,102,815). Claim 1 is cancelled for the reasons discussed above. Claims 2-4 are unanticipated by the references for the reasons discussed below regarding new claim 13 from which they now depend.

The Examiner rejected claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Chao (U.S. 4,906,589). Claim 1 is cancelled for the reasons discussed above. Claims 2-4 are unanticipated by the reference for the reasons discussed below regarding new claim 13 from which they now depend.

Newly added claim 13 is unanticipated by the Ma, Huang, Sanchez, and Chao references as there is no disclosure or suggestion in these references of forming a blocking layer over the polysilicon layer, implanting an initial dose of first conductivity type dopant prior to removing the blocking layer, implanting an additional dose of first

Apple. No. 10/023,825
Reply to Office action of 09/17/2003

conductivity type dopant after removing the blocking layer, and then, depositing a metal layer and reacting the metal layer to form a conductive silicide.

Sanchez '067 teaches an inverse T-gate structure. A polysilicon layer 36 is patterned by photoresist layer 38 and etched. The photoresist layer 38 is removed after implanting a p-type punchthrough implant. First spacers are formed and first source/drain regions 48a and 48b are formed by implanting an n-type dopant. Second spacers are then formed and source/drain regions 52a and 52b are formed by implanting an n-type dopant. While Sanchez teaches leaving the resist layer 38 in place during a p-type punch-through implant, the resist layer is removed prior to all of the n-type source/drain implants. There is no disclosure or suggestion of forming a blocking layer over the polysilicon layer, implanting an initial dose of first conductivity type dopant prior to removing the blocking layer, and implanting an additional dose of first conductivity type dopant after removing the blocking layer as required by new claim 13.

Sanchez '815 teaches a photoresist layer 38 for the polysilicon 40 etch, but removes the photoresist layer 38 prior to the source/drain implants for forming regions 42a, 42b, 46a, and 46b.

Huang teaches patterning and partially etching a polysilicon layer using a pattern 68. Pattern 68 is removed prior to any implantation. No masking layer is present over the polysilicon layer 62/72 during an implant to form regions 52. Sidewall spacers are then formed and regions 56 are implanted. In FIG. 5F, a portion of material for forming the sidewall spacers remains over the gate during the implantation of regions 56. However, claim 13 requires forming a blocking layer over the polysilicon layer, implanting an initial dose of first conductivity type dopant prior to removing the blocking layer, and implanting an additional dose of first conductivity type dopant after removing the blocking layer. This is not disclosed or suggested by Huang.

Apple. No. 10/023,825
Reply to Office action of 09/17/2003

Ma teaches several embodiments for forming a transistor. However, none of the embodiments teach forming a blocking layer over the polysilicon layer, implanting an initial dose of first conductivity type dopant prior to removing the blocking layer, and implanting an additional dose of first conductivity type dopant after removing the blocking layer as required by new claim 13.

Chao teaches forming a silicon nitride layer over a polysilicon layer. With the silicon nitride layer protecting the polysilicon layer, the LLD regions 62 and highly doped source/drain regions 64 are implanted. In contrast to the claim requirements, the blocking layer is not removing prior to implanting the additional dose of dopant to form the main source/drain regions.

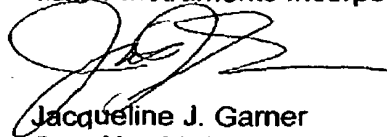
Accordingly, Applicant respectfully submits that claim 13 and the claims dependent thereon are unanticipated by the references.

The other references cited by the Examiner have been reviewed, but are not felt to come within the scope of the claims as amended.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 2-4 and 13. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Texas Instruments Incorporated



Jacqueline J. Garner

Reg. No. 36,144

Phone: (214) 532-9348

Fax: (972) 917-4418